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A NOVEL SIMPLE SCHMITT TRIGGER CIRCUIT USING CDTA AND ITS APPLICATION AS A SQUARE-TRIANGULAR WAVEFORM GENERATOR

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Abstract. In this paper current differencing transconductance amplifier (CDTA) based Schmitt trigger and a square-triangular waveform generator are presented. Square-triangular waveform generator consists of two CDTAs and less number of passive elements. In the proposed circuit, all passive elements are grounded which is advantageous in integrated circuit (IC) implementation. The circuit simulated using Cadence 180 nm CMOS technology. The performance of the proposed circuit is validated using commercially available current feedback operational amplifier (AD844 AN) and operational transconductance amplifier (LM13600); they demonstrate good agreement to the theoretical anticipation. And non-idealities are also examined.

Keywords: Current Differencing Transconductance Amplifier (CDTA), Schmitt trigger, Integrator, Square-triangular waveform generator.
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1 Introduction

Recently, current-mode (CM) active components are widely used to achieve larger dynamic range and high-bandwidth circuits with reference to operational amplifier (op-amp) based circuits. Current differencing transconductance amplifier (CDTA) is one of the current-mode CMOS based device and is found to be useful in many analog circuits. Oscillators, filters, current limiters, peak detectors etc., (Sedra & Smith, 1998; Lahiri, 2009; Biolek, 2003; Bekri & Anday, 2005; August; Biolek & Biolkova, 2005 September; Jaikla et al., 2008; Tangsrirat, 2001; Dumawipata et al., 2008) are some of the applications of CDTA.

A Schmitt trigger circuit is firstly proposed by Otto H. Schmitt in 1938 (Schmitt, 1938). Schmitt trigger circuit is extensively used in both analogue and digital domains and it is used in signal conditioning applications to eliminate noise from the signal and also it finds application in the relaxation oscillators. The first CCII+ based nonlinear design was credited to Cataldo et al, a Schmitt trigger by means of a CCII+ (Diutaldo et al., 1995). Schmitt trigger circuits employing with different active building blocks like OTAs (Kar & Sen, 2011), OTRAs (Lo et al., 2010), and current conveyors (Pal, 2009; Srinivasulu, 2011; Pal, 2009 May) have been reported in the literature. These reported circuits are suffering from the following weaknesses:

- Excessive use of active/passive components;

- Use of floating resistors, which is difficult to fabricate IC further;
- To achieve high speed and larger bandwidth, large bias currents are required which increases circuit complexity;
- Sensitive to environmental variations;
- The Clock Wise (CW) and Counter Clock Wise (CCW) hysteresis of Schmitt trigger circuit depends upon the position of switch;
- The amplitude and frequency of these realizations are mainly controlled by the passive elements.

Several square-triangular waveform generator circuits are found in the literature (Pal et al., 2009; Srinivasulu, 2011; Pal, 2009, May; Hung et al., 2005; Inchan et al., 2013 May; Minaei & Cicekoglu, 2003; Sotner et al., 2013, May; Kubanek et al., 2013, July; Kumar, 2013, December; Hou et al., 2005; Lo & Chien, 2007; Srisakul et al., 2011, May; Haque et al., 2008, April; Pandey et al., 2013; Sotner et al., 2013; Minaei & Yuce, 2012; Bothra et al., 2011, April). Most of the realizations reported earlier have been implemented using commercially available components. But in case of on-chip implementation the passive devices exhibit significant amount of variations after fabrication as it is difficult to tune the passive devices for amplitude and frequency control due to the presence of floating resistor. The proposed Schmitt trigger/square waveform generator is constructed of single active building block CDTA. The proposed square-triangular waveform generator circuit employs two CDTAs and only two passive components. The square-triangular waveform generator is constructed of Schmitt trigger and an integrator in a closed loop, and it is also advantageous in integrated circuit manufacturing, since passive components are grounded.

2 CDTA fundamentals and proposed design

2.1 Ideal CDTA

The CDTA schematic symbol and its ideal model are shown in Fig. 1(a) and 1(b). Fig. 1(b) has a pair of low impedance current inputs at *p, n* and auxiliary terminal *Z,* whose outgoing current is the difference of input currents. Here output terminals currents are equal in magnitude, but they flow in opposite directions, and the product of transconductance (gm) and the voltage at the Z terminal gives their magnitudes. Therefore, this active element can be characterised by the following equations

$$V_p = V_n = 0, \;\; I_Z = I_p - I_n, \;\; I_{X+} = g_m V_Z, \;\; I_{X-} = -g_m V_Z, \tag{1}$$

where $V_Z = I_Z$. Z_Z and Z_Z is the external impedance connected to Z- terminal of CDTA. CDTA is a combination of a Current Differencing Unit (CDU) and dual output-operational transconductance amplifier (DO-OTA) shown in Fig. 2. Ideally, the DO-OTA is a voltage-controlled current source and can be described by $I_X = g_m(V_+ - V_-)$ where I_X is the output current, and V_+ and V_- denote the non-inverting and inverting input voltage of the DO-OTA, respectively. Note that g_m is a function of the bias current, given in equation (2). When one of its input terminal is said to be grounded (e.g., $V_- = 0V$). With dual output availability, $I_{X^+} = -I_{X^-}$ condition is assumed.

A possible CMOS-based CDTA circuit is shown in Fig. 2 and transistor aspect ratios are indicated in Table 1. DOTA's transconductance g_m is controllable via its bias current I_{b3}, where g_m is given by

$$g_m = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{b3}}. \tag{2}$$

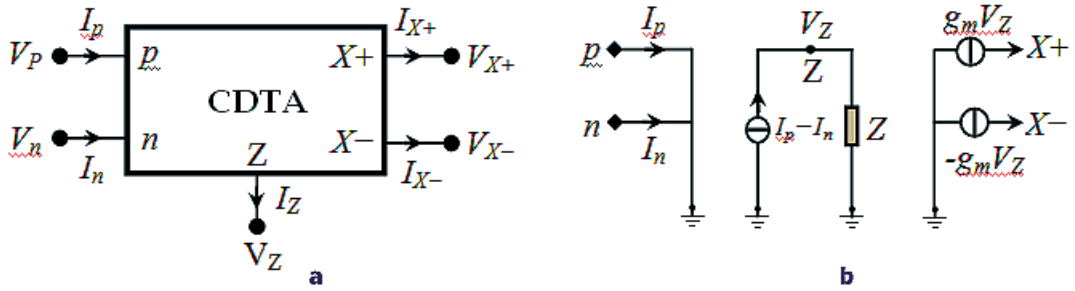

Figure 1: (a) Symbol for CDTA, (b) Ideal model of CDTA

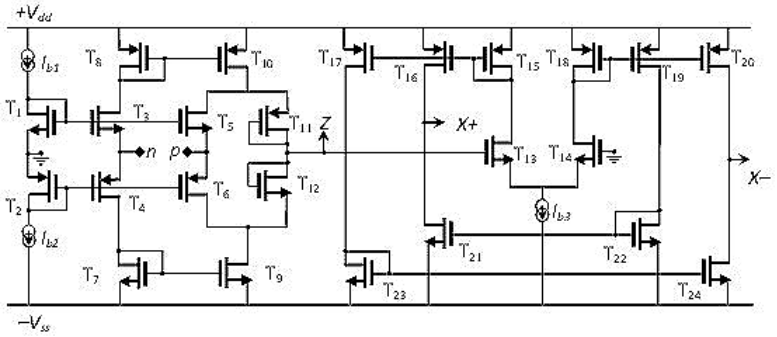

Figure 2: Device level presentation of the CDTA (Keskin & Biolek, 2006)

Table 1: Transistor aspect ratios of Fig. 2

Transistor	W (µm)	L (µm)
T_1-T_6	10	0.9
T_7- T_{10}	5	1.0
T_{11}, T_{12}	20	2.0
T_{13}, T_{14}	16	1.0
T_{15}-T_{20}	6	1.0
T_{21}-T_{24}	4	1.0

2.2 Proposed Schmitt trigger circuit

The proposed Schmitt trigger circuit comprises of single active building block CDTA shown in Fig. 3 and the circuit operation is as follows. Initially, it is assumed that the input V_{in} is positive rising sine waveform (from $-V_{in}$ to $+V_{in}$ and accompanying current at port 'n' of CDTA is rising from $-I_i$ to $+I_i$ and also current at port Z also rise from $-I_Z$ to $+I_Z$. Consequently current at output node 'X_+' rises from $-I_{X+}$ to $+I_{X+}$. At this point the output voltage is $-V_0$ (with previous cycle). When the input current $+I_i(= V_{in}/R_S)$ is greater than $(R_s(1-g_mR)/g+mR)V_0$, the current direction at output port 'X' is $-I_{X+}$ and the output voltage is $-V_0$. This is known as Upper Triggering Point (UTP). The output voltage $-V_0$ remains negative until the input sine waveform reaches a value of $-I_i[\geq -(V_{in}/R_S)]$ at port 'n'.

When the input current $-I_i$ at port 'n' is greater than $-(R_s(1-g_mR)/g_mR)V_0$ the current direction at the output port 'X_+' is $+I_{X+}$ and the output voltage is $+V_0$. This is known as Lower Triggering Point (LTP). While the output voltage $+V_0$ remain negative until the input sine waveform reaches a value of $+I_i[\geq -(V_{in}/R_S]$ at port 'n'. The cycle repeats and generates

a square waveform. The simulation results are shown in Fig. 4 and Fig. 5. The hardware implementation of Fig. 3 is obtained with the schematic in Fig. 11 and the measured results are shown in Fig. 6 and Fig. 7. The transfer function of the Fig 3 is given by:

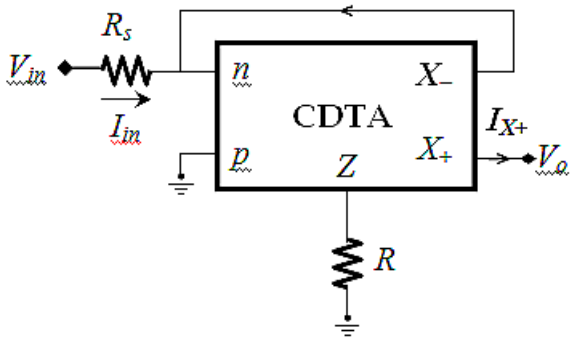

Figure 3: Proposed Schmitt trigger using CDTA

$$\frac{V_o}{I_{in}} = -\frac{g_m R}{1 - g_m R} \ (or) \ \frac{V_o}{V_{in}} = -\frac{g_m R}{R_S(1 - g_m R)}. \tag{3}$$

Hence the UTP and LTP equations for the proposed circuit of Fig. 3 are given by

$$UTP = \frac{R_S(1 - g_m R)}{g_m R}, \tag{4}$$

$$LTP = -\frac{R_S(1 - g_m R)}{g_m R}. \tag{5}$$

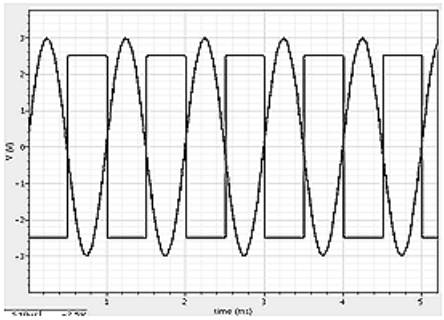

Figure 4: Typical sine input and square output waveform

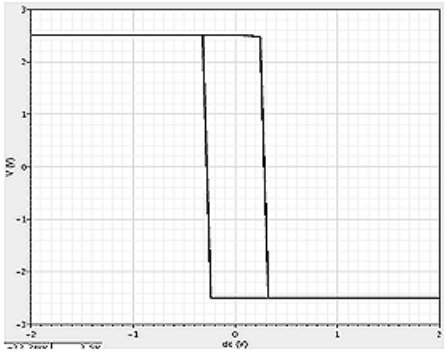

Figure 5: Simulated DC transfer characteristic of Fig. 3 Schmitt trigger

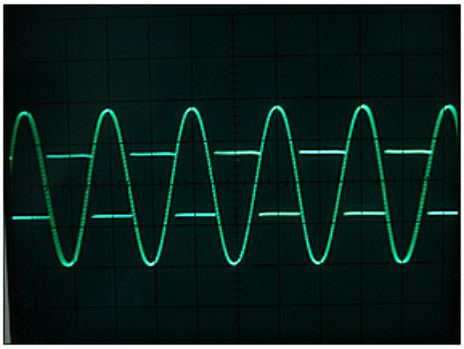

Figure 6: Typical hardware implemented sine input and square output waveform
Scale: X-axis 1 ms/div and Y-axis 5V/div (square waveform), Y-axis 1V/div (sine waveform)

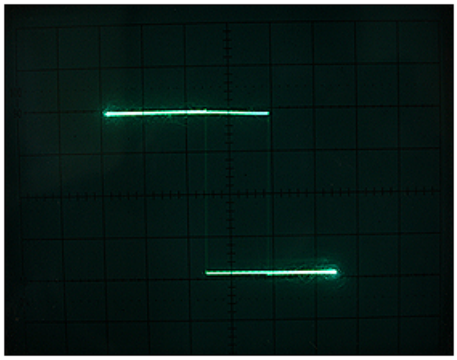

Figure 7: Hardware implemented transfer characteristic of Fig. 3 Schmitt trigger

2.3 Proposed square-triangular waveform generator

The circuit diagram of the proposed square-triangular waveform generator is presented in Fig. 8. By considering the ideal terminal characteristics involved in CDTA referred in equation (1) and (2) and the relevant notations appearing in Fig. 8, the mathematical representation proposed is as follows:

$$I_{X2-} = -g_{m2}V_{Z2}, \tag{6}$$

$$V_{Z2} = I_{Z2}Z_{Z2}, \tag{7}$$

$$I_{Z2} = I_{p2}, \tag{8}$$

$$I_{X1+} = g_{m1}V_{Z1}, \tag{9}$$

$$I_{X1+} = I_{Z2}, \tag{10}$$

$$V_0 = V_{Z1} = I_{Z1}R, \tag{11}$$

$$I_{Z1} = -I_{n_1}. \tag{12}$$

From the above relations and from the ideal behavior of CDTA given in (1) and (2) it is easy to derive the characteristic equation of Fig. 8 in the form

$$sC(1 - g_{m1}R) + g_{m1}g_{m2}R = 0. \tag{13}$$

with $s = j\omega$, where ω is the angular frequency in rad/s, from the above equation (13), the oscillation frequency (f) is written as:

$$f = \frac{g_{m1}g_{m2}R}{2\,\pi\,C(g_{m1}R-1)}, \tag{14}$$

Thus the time period (T) is expressed as:

$$T = \frac{2\pi C(g_{m1}R-1)}{g_{m1}g_{m2}R}, \tag{15}$$

where g_{m1} and g_{m2} are transconductances of $CDTA_1$ and $CDTA_2$, respectively.

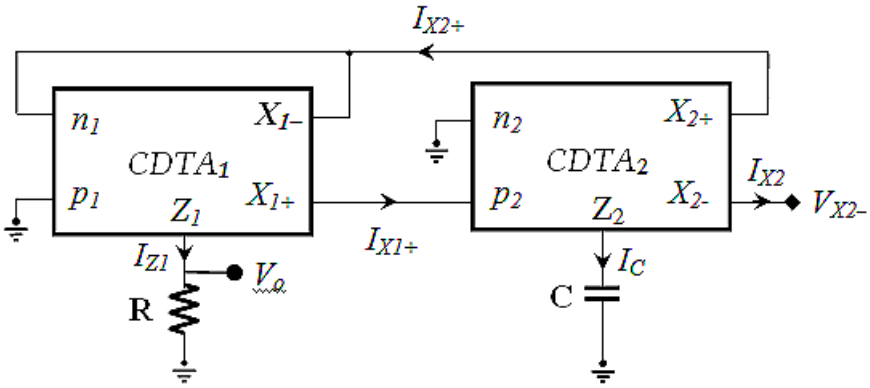

Figure 8: Circuit diagram of the proposed square-triangular waveform generator

3 Non-ideal analysis

In the real world, the performance of proposed circuits may deviate from the ideal case, so parameters of a practical model of a CDTA including some non-idealities are taken into account. In this analysis the non-ideal case of CDTA is characterized by

$$V_p = V_n = 0,\ I_Z = \alpha_p I_p - \alpha_n I_n,\ I_{X+} = \beta\ g_m V_Z,\ I_{x-} = -\beta\ g_m V_Z, \tag{16}$$

where a_p, a_n are the parasitic current gains between the $p-Z, n-Z$ terminals of the CDTA, β is the transconductance inaccuracy factor from terminals Z to X of the CDTA respectively. Which are slightly differing from their ideal unity values by current-tracking errors, and their absolute values being much less than one. The non-ideal representation of CDTA is shown Fig. 9.

Let resistors R_p, R_n, R_Z, R_X and capacitor C_X, C_Z be the parasitic impedances of terminals p, n, Z and X of the CDTA respectively. Considering $C >> C_Z, R << R_Z$ and by using equation (16) and also by repeating the complete analysis as shown in section 2.3, with the parameters α_p, α_n and β, modified relation for the oscillation frequency (f) is written as:

$$f = \frac{\beta_1\beta_2\alpha_{n1}\alpha_{p2}\,g_{m1}g_{m2}\,R}{2\,\pi\,C\,(\beta_1\alpha_{n1}g_{m1}R-1)}. \tag{17}$$

Thus the time period (T) is expressed as:

$$T = \frac{2\,\pi\,C\,(\beta_1\alpha_{n1}g_{m1}R-1)}{\beta_1\beta_2\alpha_{n1}\alpha_{p2}\,g_{m1}g_{m2}\,R}. \tag{18}$$

It can be easily verified that, the equation (17) and (18) reduces to equation (14) and (15) as expected, for ideal CDTA when $\alpha_{n1} = \alpha_{p2} = 1$ and $\beta_1 = \beta_2 = 1$.

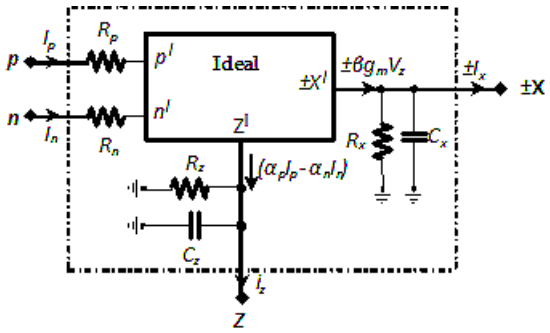

Figure 9: Simplified equivalent circuit of the non-ideal CDTA

4 Measured results and comparison

To validate the theoretical analysis of the proposed Schmitt trigger circuit and square-triangular waveform generator circuit, they are simulated using Cadence $180nm$ CMOS technology. The CMOS based CDTA internal structure used in the simulation is shown in Fig. 2. The proposed square-triangular waveform generator circuit shown in Fig. 8 is designed with supply rail voltage $\pm 2.5V$, bias currents $I_{b1} = I_{b2} = 85\mu A, I_{bias} = I_{b3} = 480\mu A, C = 50pF$ and $R = 10k\Omega$. Similarly for the Schmitt trigger circuit shown in Fig. 3 the supply voltage and bias currents are same but passive components are chosen as $R_s = 1k\Omega, R = 10k\Omega$ and $V_{in} = 3V_p$. CDTA's transconductance is controlled by bias current I_{b3}. When the bias current (I_{b3}) is $480\mu A$, then the transconductance (g_m) is 1.43 m-mho. As both CDTAs of Fig. 8 are tuned simultaneously for same bias currents, hence $g_{m1} = g_{m2} = g_m$. The simulation result of square-triangular waveform generator is shown in Fig. 10. The simulated time period of Fig. 8 is $0.74\mu s$ and from (15) calculated time period is $0.22\mu s$.

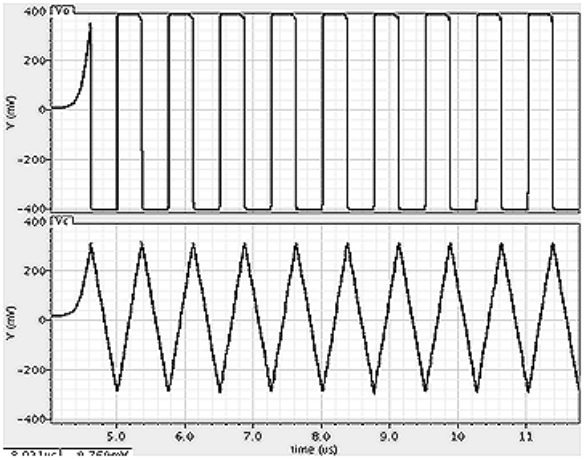

Figure 10: Typical square/triangular waveform of Fig. 8

The tunability for the grounded capacitor C is next tested for the configuration. For this the passive component is chosen as $R = 10k\Omega$, and bias current $I_{bias} = 480\mu A$, power supply rail $\pm 2.5V$ and the capacitor C is varied from $40pF$ to $500pF$. Similarly, for resistor R, the selected parameters are $C = 200pF$ and $I_{bias} = 480\mu A$. Resistor R is varied from $1k\Omega$ to $10k\Omega$. As the graphs obtained from the simulated results more or less replicates the measured ones, which are already presented below, so they are not included to avoid the repetition. The optimized layout of Fig.8 is shown in Fig.14.

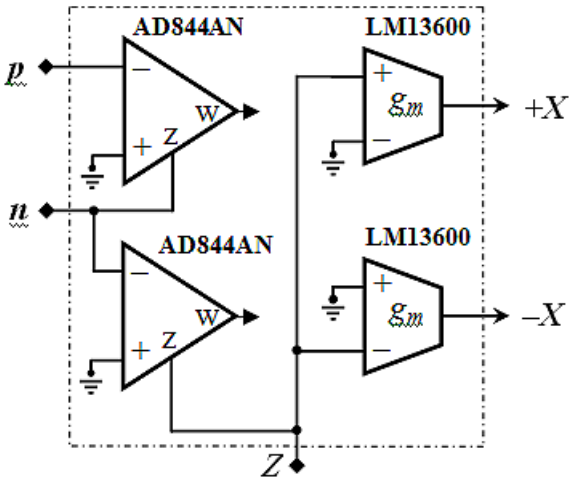

Figure 11: Implementation of CDTA using commercially available ICs AD844AN and LM13600

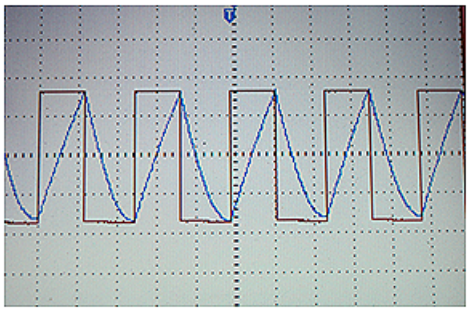

Figure 12: Experimentally observed square/triangular waveform from the built circuit as per Figure 8. Scale: X-axis $1ms/div$ & Y-axis $5V/div$

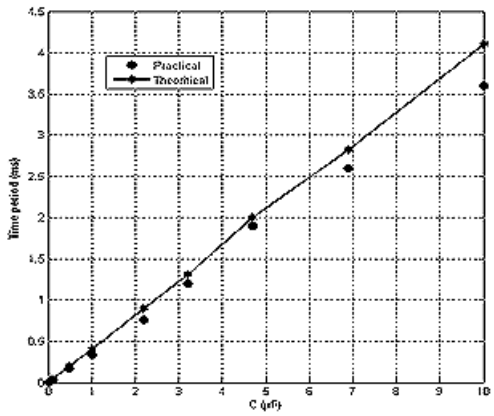

Figure 13: Variation of time period against capacitor C

The behavior of CDTA is obtained with the schematic in Fig.11 (Jin & Wang, 2014).

Table 2: Comparison with candidate designs

Ref. No.	Name of the Active Component (Number used)		Total no. of Passive Components	Number of components grounded	Hardware Results with Commercial ICs	Frequency Range
(Pal *et al.*, 2009)	CCII (2)		4	1	Yes	250 kHz
(Srinivasulu, 2011)	CCII (3)		7	5	Yes	150 kHz
(Pal *et al.*, 2009, May)	CCII (3)		7	3	Yes	400 kHz
(Hung *et al.*, 2005)	OTA (3)		3	3	Yes	900 kHz
(Inchan *et al.*, 2013)	MO-CFTA (2)		1	1	No, (Simulated)	500 kHz
(Sotner *et al.*, 2013)	CG-CDVA (1)		2	1	No, (Simulated)	0.56 MHz to 11.39 MHz
(Kubanek *et al.*, 2013)	MO-CCDVCC (1)		2	2	No, (Simulated)	590 kHz
(Kumar, 2013)	Op-amp (2)		4	None	Yes	462 kHz
(Hou *et al.*, 2005)	OTRA (1)	Fig. 2a	3	None	Yes	1 MHz
		Fig. 2b	4 & 2 Diodes	None	Yes	-
(Lo *et al.*, 2007)	OTRA (2)		4 & 2 Switches	None	Yes	1 MHz
(Srisakul *et al.*, 2011)	MO-CCCCTA (2)		1	1	No, (Simulated)	400 kHz
(Haque *et al.*, 2008)	CFOA (2)		5	1	No, (Simulated)	9.4 MHz to 15 MHz
(Pandey *et al.*, 2013)	CDBA (1)	Fig. 2	3	1	Yes	824 kHz
		Fig. 4	4 & 2 Diodes	1	Yes	-
		Fig. 5	4	1	Yes	-
(Sotner *et al.*, 2013)	DO-VDBA (1), FB-VDBA (1)		3	3	No, (Simulated)	211 kHz to 2.83 MHz
(Shahram *et al.*,2012)	DVC C (2)		3	3	Yes	-
(Shahram *et al.*, 2012)	CFOA (2)		4	3	Yes	400 kHz
(Bothra *et al.*, 2011)	OTRA (2)		5	None	No, (Simulated)	2.6 MHz
Fig. 6	Proposed circuit with CDTA (2)		2	2	Yes	600 kHz (Simulated) 410 kHz, (Hardware)

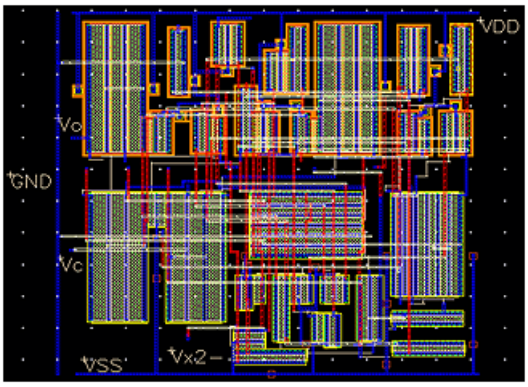

Figure 14: RC extracted layout of proposed square-triangular waveform generator

Commercially available CDTA as monolithic ICs AD844 AN and LM13600 are used to fabricate the design of Fig.3 and Fig.8. Fig.3 is designed with a supply rail voltage of $\pm 4V$, bias

current $I_{bias} = 700\mu A$ and passive components are chosen as $R = 10k\Omega$ and $R_s = 1k\Omega$. The measured results of Fig. 3 are shown in Fig.6 and Fig.7 for an applied sine input waveform of $2Vp$. In a similar way Fig.8 is designed with a power supply rail typically $\pm 9V$ and bias current $I_{bias} = 700\mu A$. The transconductance g_m is 15 m-mho for the bias current (I_{bias}) of $700\mu A$ (`www.alldatasheets.com`).

A typical square/triangular waveform from the oscilloscope screen is shown in Fig. 12 which has been obtained for a power supply rail typically $\pm 9V$, bias current $I_{bias} = 700\mu A$ and for component values $R = 2.7k\Omega$ and $C = 4.7\mu F$. The measured time period is 2.5 ms as is observed from Fig.12 closely coincides with the predicted time period of $2.04ms$ obtained from (15) by using ideal implementation of CDTA (Fig.11). The tunability of the configuration is tested for capacitor C. For this the passive component is chosen as $R = 2.7k\Omega$, and the capacitor C varied from $5nF$ to $10\mu F$. The tunability for the range from $200Hz$ to $410kHz$ can be verified from the plot given in Fig. 13. Comparison of proposed square-triangular waveform generator with various conventional waveform generators is given in Table 2.

5 Conclusion

A simple Schmitt trigger and square-triangular waveform generator circuits are proposed using CDTA as an active element. The proposed circuit generates both square and triangular waveforms of 410 kHz frequency. The analysis and the measured results involved exhibit close matching with those for the theoretical analysis. Square-triangular waveform generator circuit is more advantageous i) the circuit consist of only one grounded capacitor which is advantage in Integrated Circuit (IC) implementation. ii) The oscillation frequency is made adjustable by using voltage-controlled elements (MOSFETs), since the resistor in the circuit is grounded iii) The circuit consists of only two passive components. Tunability of grounded components is an attractive feature of the design as it provides an easy option for digital control by programmable switched capacitor/resistor array. With the above advantages it is expected that the proposed circuit is useful in various analogue signal processing applications and in instrumentation systems.

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